OptiSPICE

Tutorials - Electrical Circuit Examples

Opto-Electronic Circuit Design Software

Version 5.2

OptiSPICE

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Tutorials - Electrical Circuit Examples

This tutorial covers typical electrical circuits and how they can be designed and simulated with OptiSPICE. It includes the following examples:

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- A ***Single stage common emitter amplifier*** using an NPN transistor
- An ***XOR gate*** designed at the transistor level.
- Examples of ***CMOS Buffer*** and ***CMOS Inverter*** designs
- An example of a circuit based on a vendor specified Netlist file (National Semiconductor **LM324 Circuit Block**)
- A macro-model circuit for the industry standard ***µA-741 Operational Amplifier***

Half Wave Rectifier

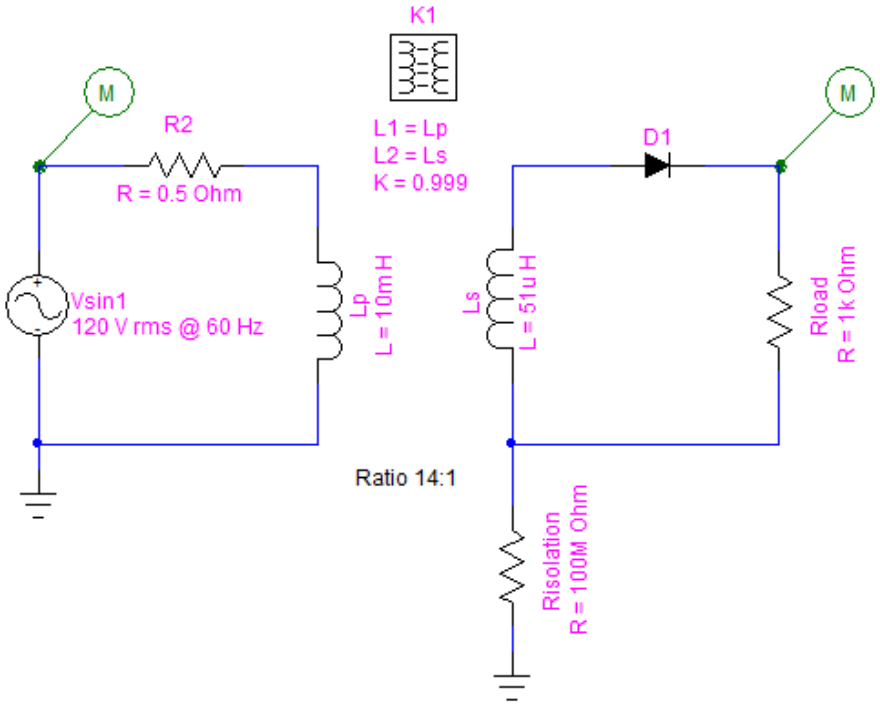
In this tutorial, we demonstrate a half-wave rectifier using a transformer and a diode.

Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\Half Wave Rectifier**Wave Rectifier.osch***

The transformer is built using two inductors and a mutual inductor both located in the **electrical** library. The inductance of the first and second inductor are set to 10 mH and 51 uH respectively. The mutual inductor defines the coupling ratio between the two which is 0.999 in this example.

Figure 1 shows the setup for the half-wave rectifier. The input is a sine wave at 60 Hz with 120 Vrms amplitude. The diode is located in the **electrical** library and has the model of D1N4148. We have put a 1 KOhm resistor as a load.

Figure 1 Layout of the half-wave rectifier

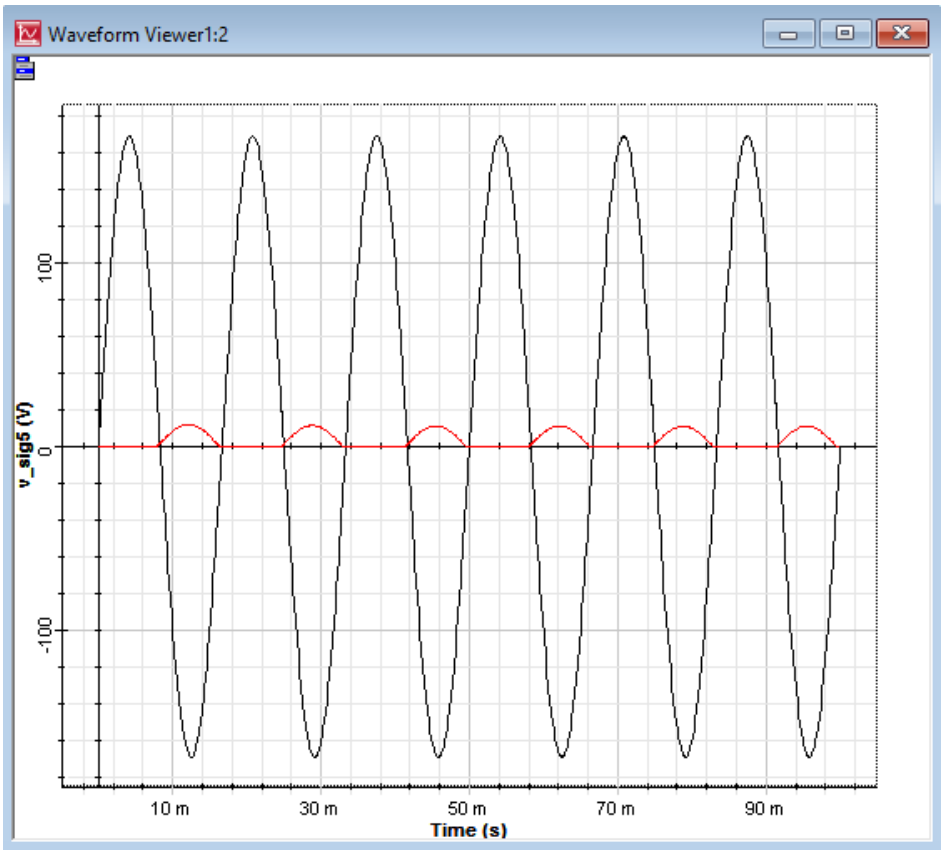


In this example, we put a probe on the input signal and one for the rectified signal.

After saving the project, in the Analysis tab, choose Setup. In this example we do Transient analysis for 100 ms with 0.05 ms step size.

After running the simulation, launch Waveform Viewer to view the results (Figure 2).

Figure 2 Sinusoidal signal and the half-wave rectified output



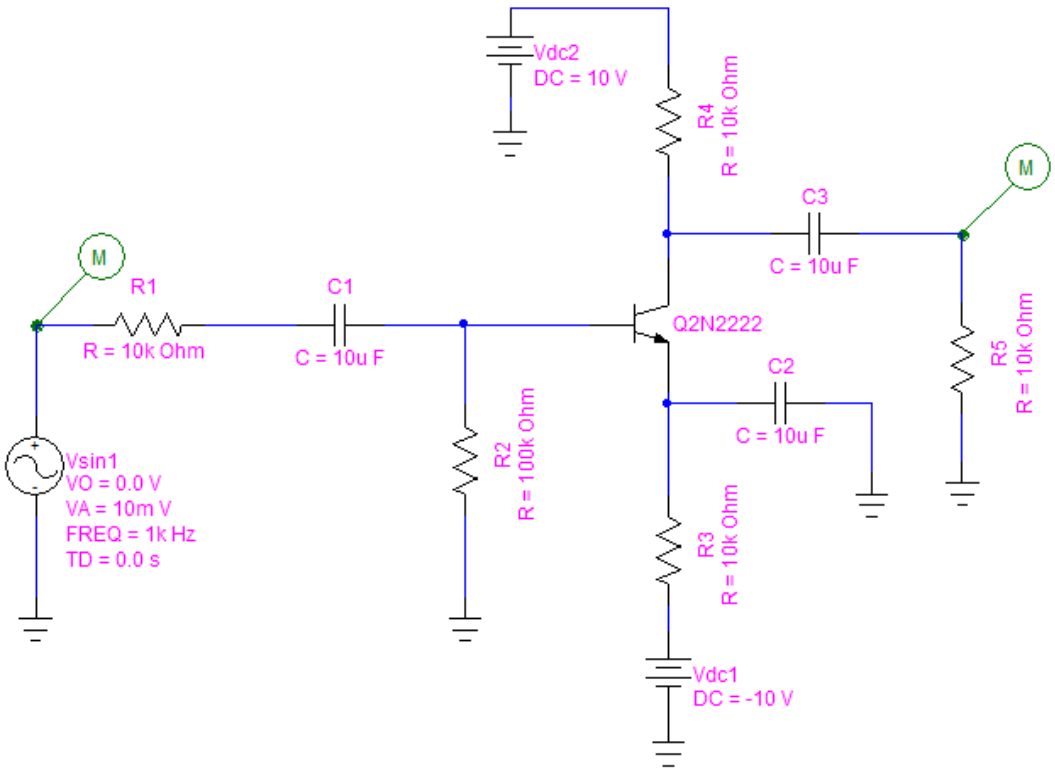
Single Stage Common Emitter Amplifier

In this tutorial, we demonstrate a single stage common emitter amplifier using an NPN transistor.

Sample: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\Single Stage CE Amplifier**Single Stage Common Emitter Amplifier.osch

The NPN transistor is located in the **Electrical** library. The transistor has the model of Q2N2222. Figure 3 shows the simulation layout. The input is a sine wave at 1 kHz with 10 mV peak amplitude. The transistor is biased using two DC power supplies providing 10 volts, and the load is a 10 KOhm resistor.

Figure 3 Layout of Single Stage Common Emitter Amplifier

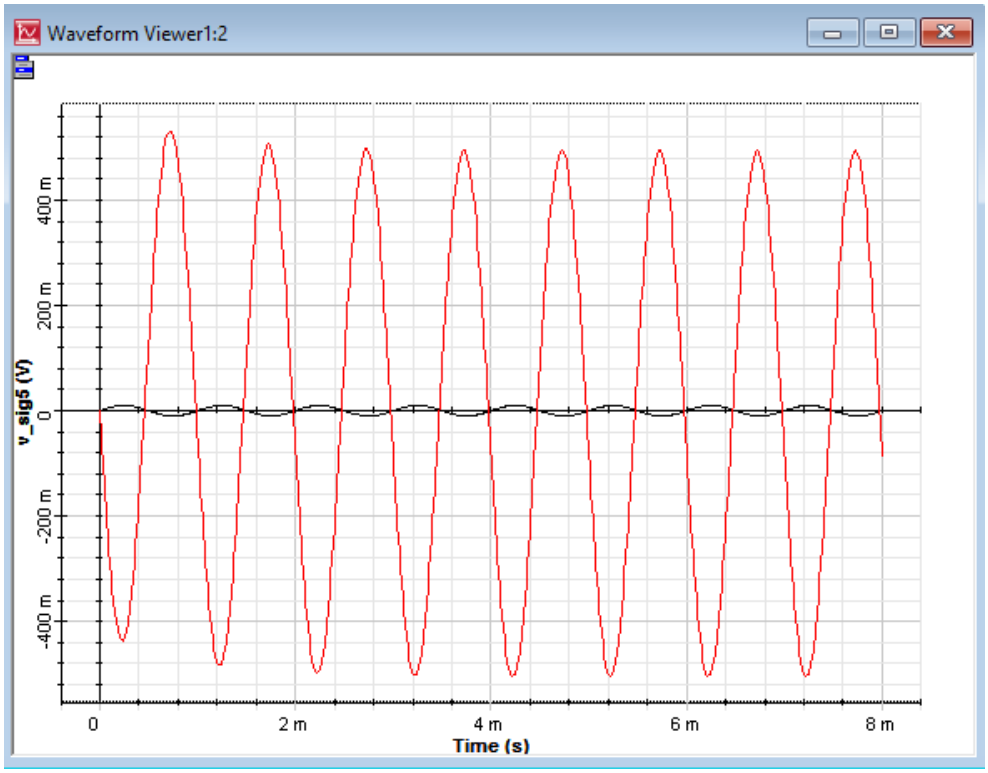


In this example, we put a probe on the input signal and one for the amplified signal.

After saving the project, in the Analysis tab, choose Setup. In this example we do Transient analysis for 8 ms with 0.01 ms step size.

After running the simulation, launch Waveform Viewer to view the results. Figure 4 shows the input sinusoidal signal and the amplified output signal. The peak amplitude of the output signal is 495 mV.

Figure 4 Sinusoidal input signal and the amplified output



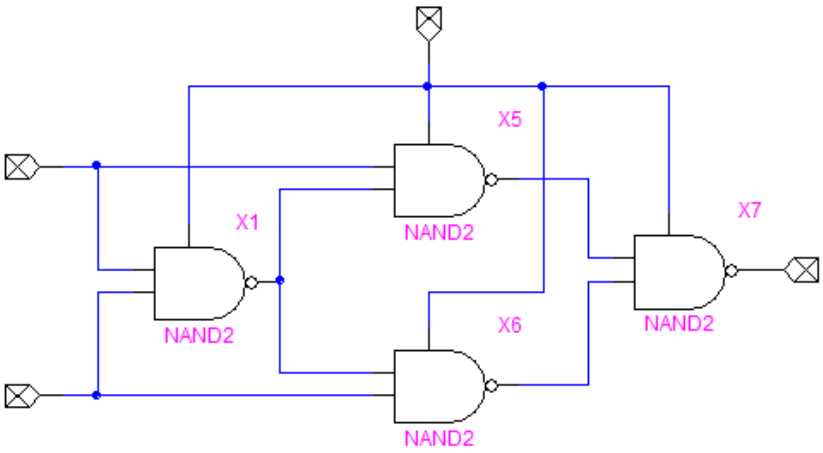
XOR Gate

In this tutorial, we use the OptiSPICE library to build an XOR gate at the transistor level.

Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\XOR Gate**XOR Gate.osch***

In this example we used NAND gates to build the XOR gate. Figure 5 shows the layout of the XOR gate. The two ports at the left side are the inputs of the XOR gate and the one on the top is the bias voltage.

Figure 5 Building XOR gate using NAND gates



In order to build a CMOS NAND gate, we used P-channel and N-channel MOSFET transistors located in the **electrical** library. Figure 6 shows the schematics of the CMOS NAND gate.

In order to analyze the XOR gate, we use the setup as shown in Figure 7. The two inputs to the XOR gate are two voltage pulse sources that generate trapezoidal pulse waveform for transient analysis. The Bias is provided using a DC voltage source with 5 volts. The output of the XOR gate is grounded with a 0.1 pF capacitor. In this example, we put probes on two input signals and the output of the XOR gate.

Figure 6 CMOS NAND gate

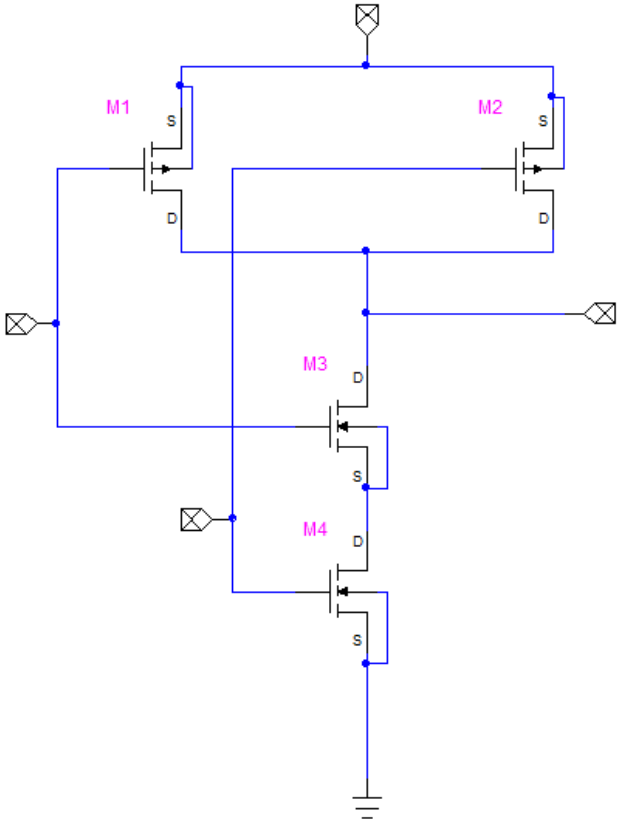
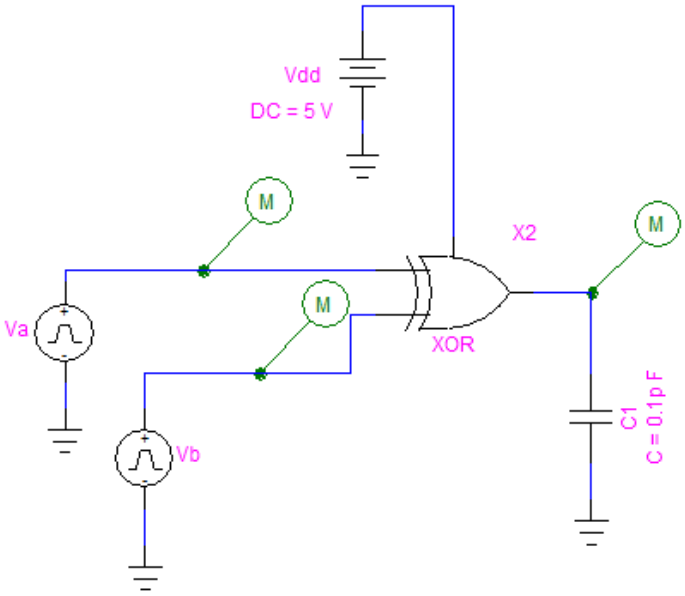


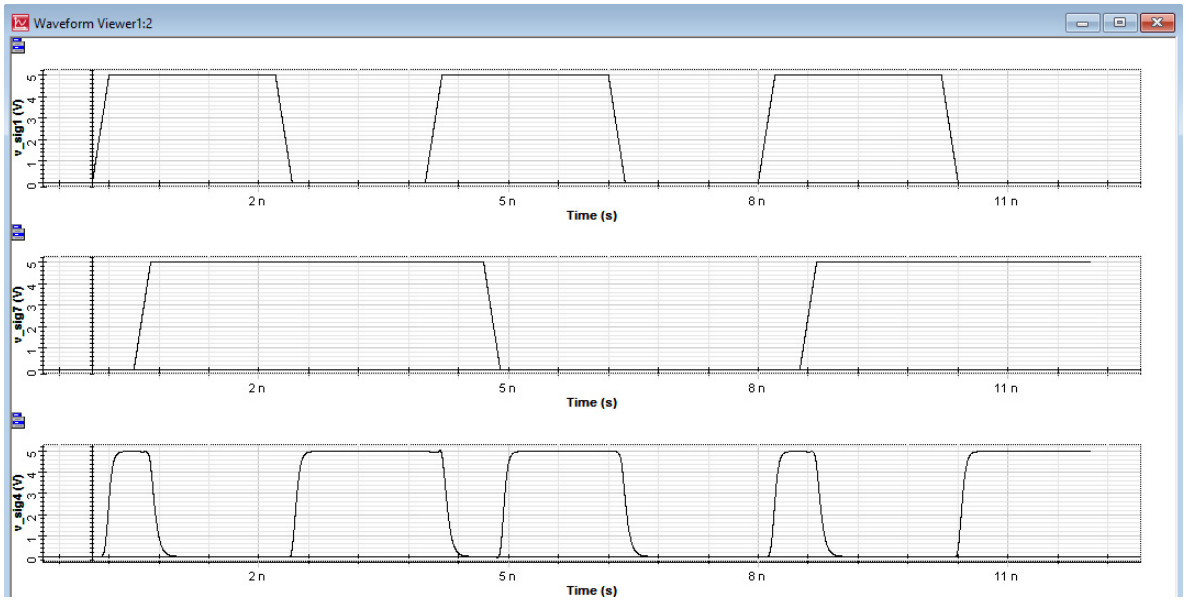
Figure 7 Setup to Analyze XOR Gate



In this example, we perform transient analysis on the XOR gate. The time duration is 12 ns and the step size is 0.001 ns.

After running the simulation, launch Waveform Viewer to view the results. Figure 8 shows the two inputs to the XOR gate and the output in time domain.

Figure 8 Input pulses to the XOR gate and the output

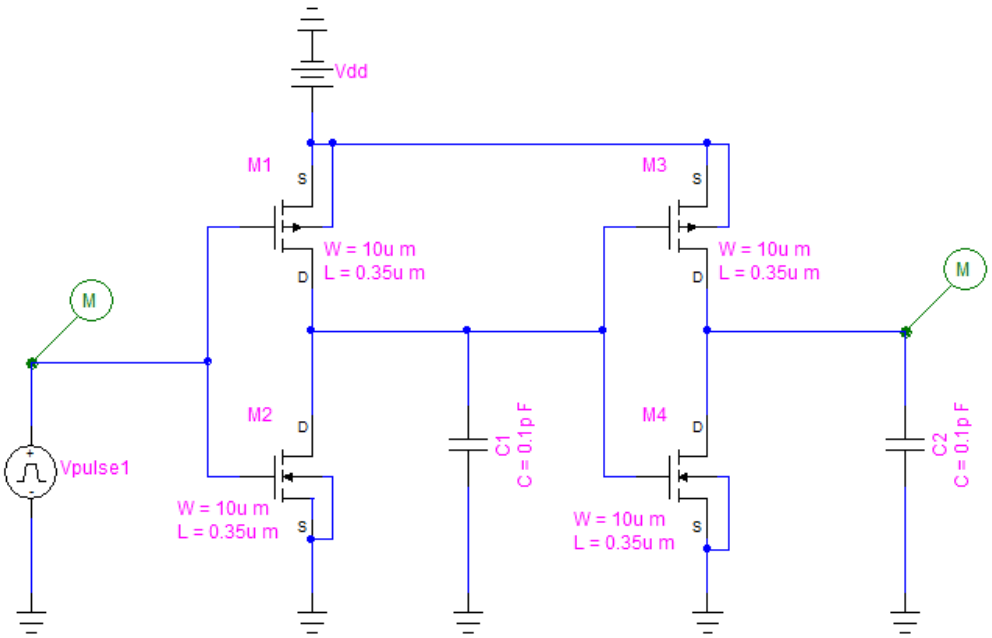


CMOS Buffer

A buffer is used to delay a signal for a short period in digital circuits. The following is a two stage CMOS buffer created by cascading two CMOS inverters.

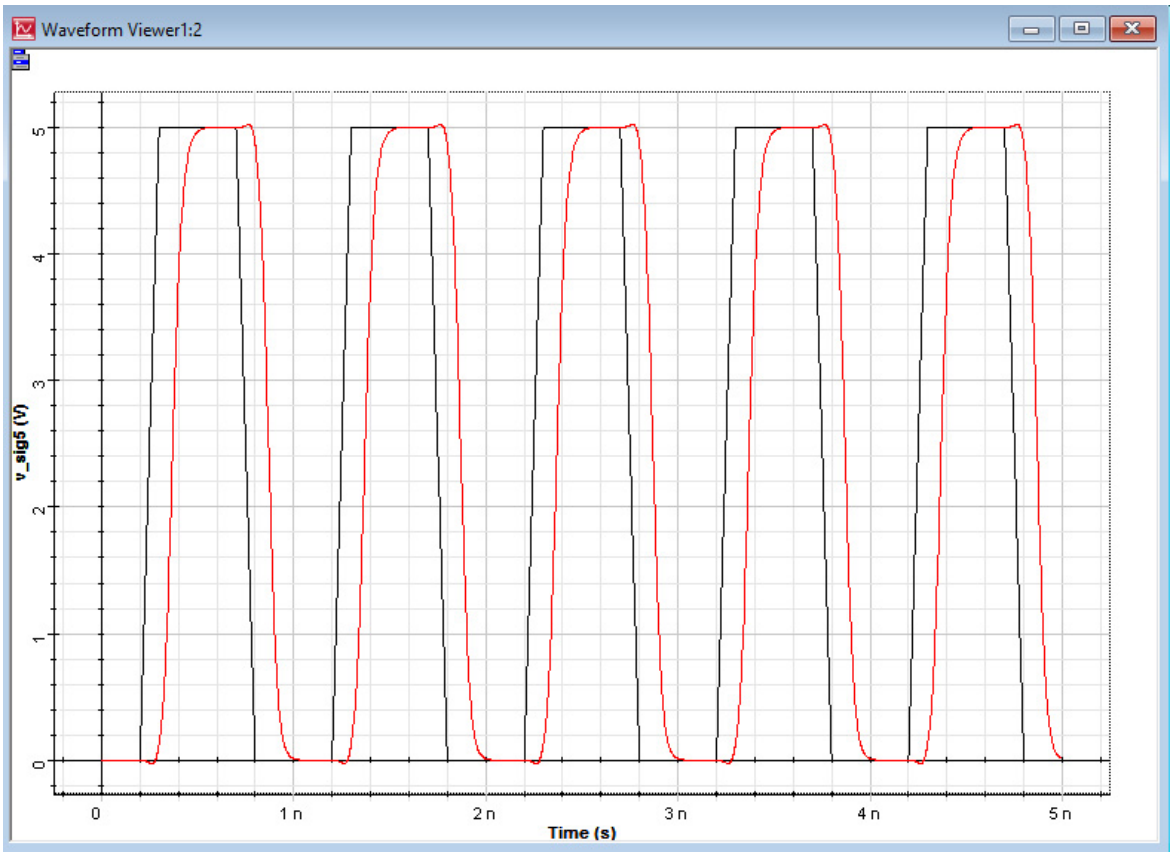
Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\CMOS Buffer**CMOS Buffer.osch***

Figure 9 Schematics for CMOS Buffer



A pulse input with peak voltage of 5V with rise and fall time of 0.1 ns is applied at the input. All the transistors are modeled with BSIM3 models. The output has a capacitance of 0.01 pF. Voltage probes are placed on both input and output nodes. Figure 10 shows input (blue solid) and output (red dashed) voltage waveforms where you can observe the small delay for the output.

Figure 10 CMOS buffer input and output comparison

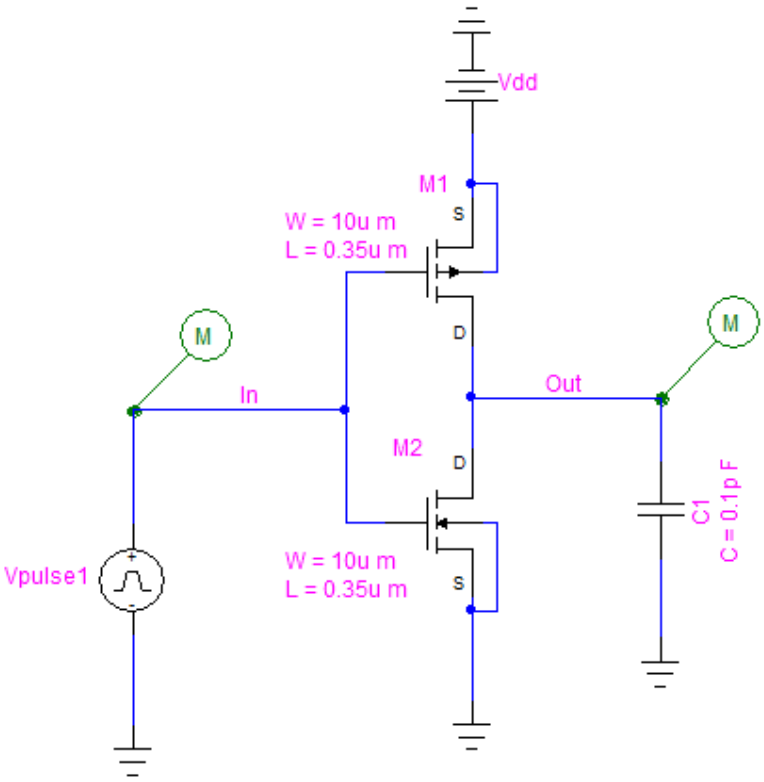


CMOS Inverter

Complementary Metal Oxide Semiconductor (CMOS) is a technology where complementary and symmetrical pairs of p-type and n-type MOSFETs are used together for integrated circuit design. Due to the complementary nature of the operations of p-type and n-type MOSFETs it inverts the logic level of the input at the output.

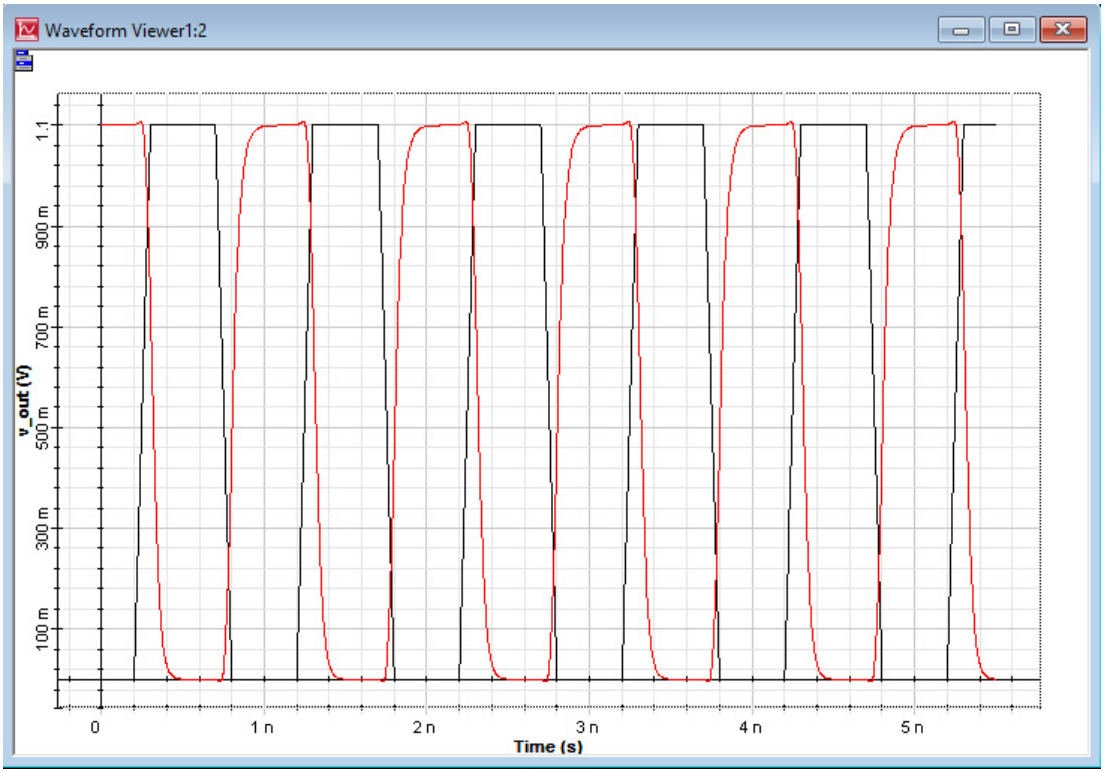
Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\CMOS Inverter**CMOS Inverter.osch***

Figure 11 Schematics for CMOS Inverter



A pulse input with peak voltage of 5V with rise and fall time of 0.1 ns is applied at the input. The Mp and Mn are p-type and n-type MOSFETs respectively. BSIM3 (Berkeley Short-channel IGFET Model Level 3) model types are used for both MOS transistors. The output has a capacitance of 0.01 pF. Voltage probes are placed on both input and output nodes. Figure 12 shows the input and output voltage waveforms for the transient analysis.

Figure 12 Input (black) and output (red) voltages



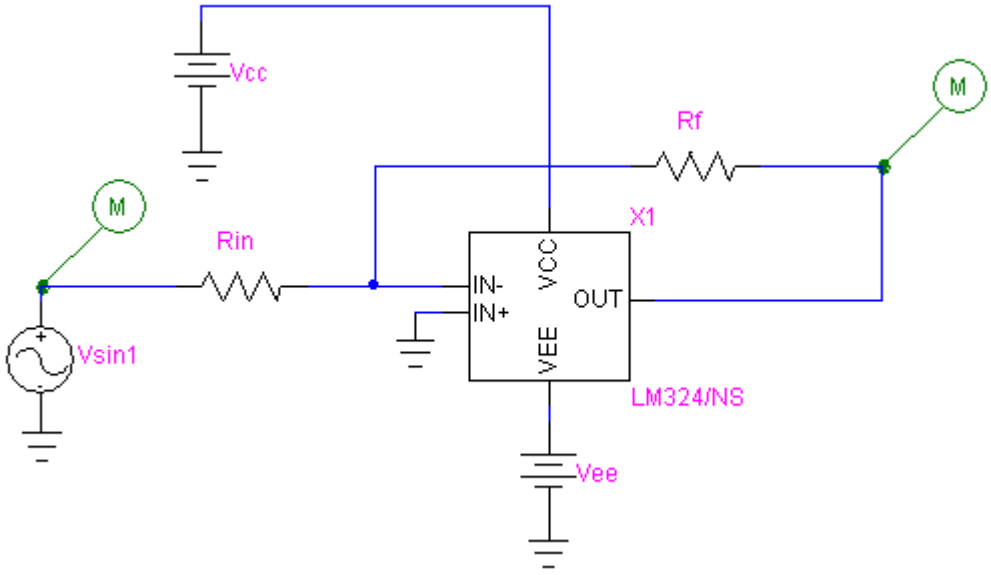
LM324 Circuit

This example demonstrates the use of a vendor provided Netlist in OptiSPICE simulation.

Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\LM324 Circuit Block**LM324 Circuit Block.osch***

The LM324 is an operational amplifier by National Semiconductor. In this example, we represent the provided Netlist as a circuit block with the necessary pins and apply a sinusoidal input as shown by Figure 13.

Figure 13 Use of LM324 Circuit Block



The LM324 Netlist is provided in the form of a SPICE sub circuit and we represent it using the Subcircuit Block (using ***Options > Subcircuit > Create Subcircuit Block***) in the Schematics with pins corresponding to the LM324 sub circuit definition statement. The Netlist is then associated to the block symbol with the use of model editor. The Netlist statement can be accessed by clicking ‘Parameters’ on the pop-up menu for this device symbol and then by launching the model editor. Figure 14 shows the LM324 Netlist in the OptiSPICE model editor.

Figure 15 shows the input and output voltage waveforms where you can see the output voltage is inverted with the gain of 10.

Figure 14 LM324 Netlist provided with Model Editor

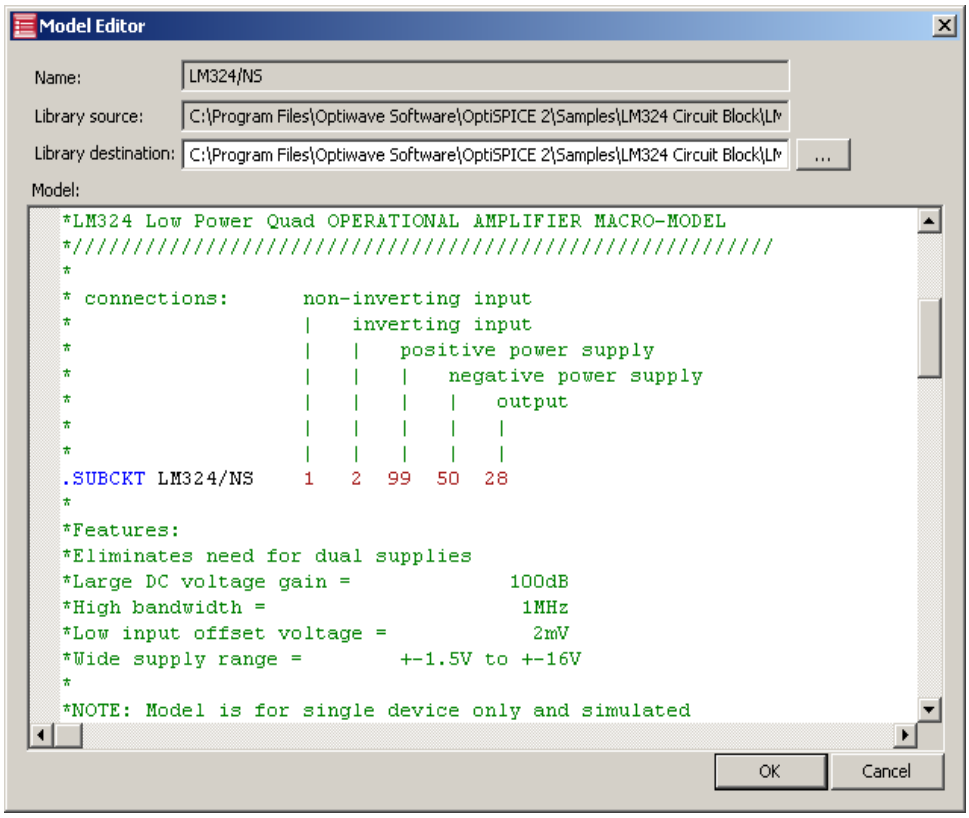
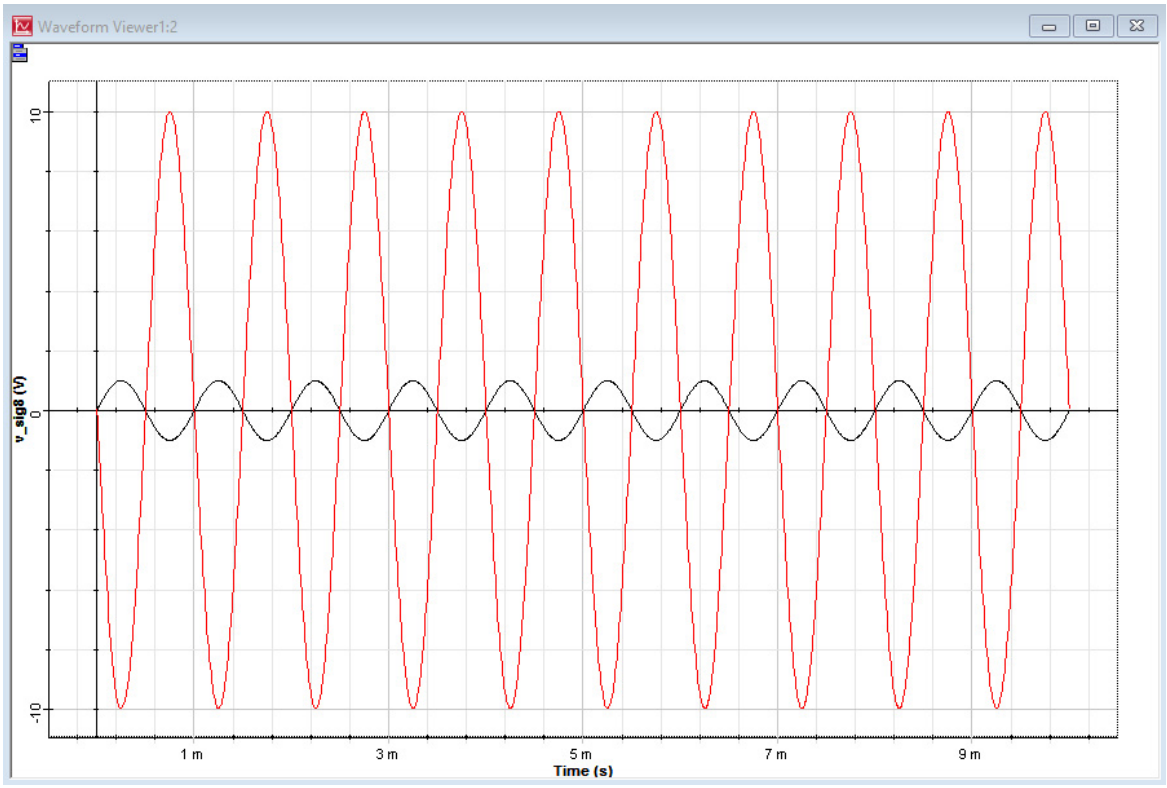


Figure 15 .Input (black) and output (red) voltages



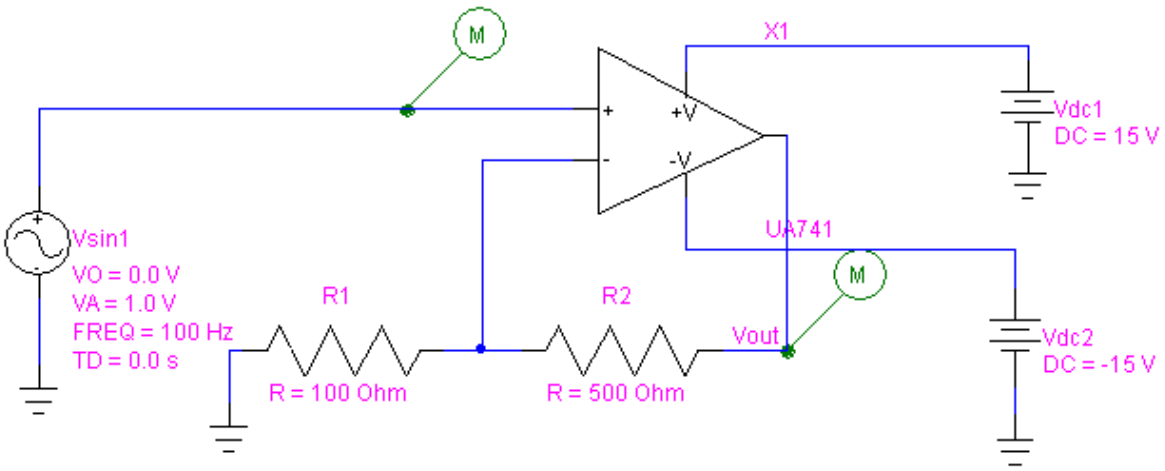
UA741 Non Inverting Amplifier

In this example, a macro-model circuit for the commonly available industry standard µA-741 operational amplifier is analyzed with a sinusoidal input voltage.

Sample location: *OptiSPICE 5.2 Samples\Circuit examples\Electrical circuits\UA741 OpAmp**UA741 Non Inverting.osch***

The external circuitry for the amplifier is connected such that it produces a non-inverting voltage at the output.

Figure 16 Top level circuit using µA-741 operational amplifier



Here the operational amplifier is represented by the sub-circuit block UA741 in the schematics. Double clicking on it shows the internals of the op-amp as given below. The sub-circuit internally contains other sub-circuit blocks for bias, input stage, intermediate stage, and output stage.

Figure 17 Figure 2 – UA741 Subcircuit

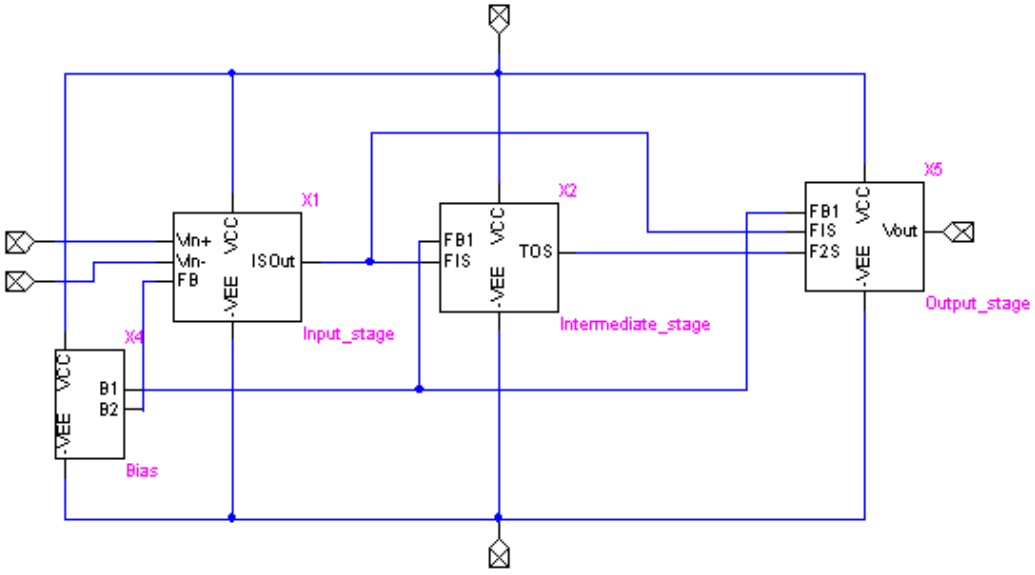
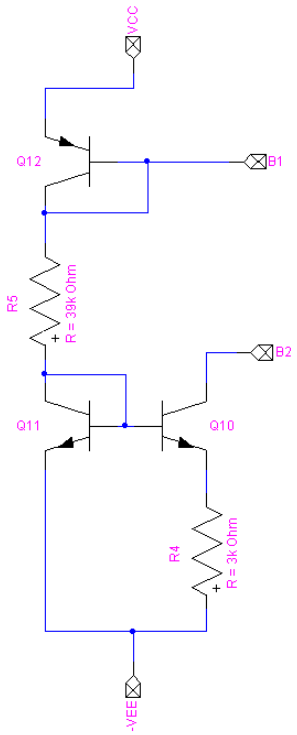
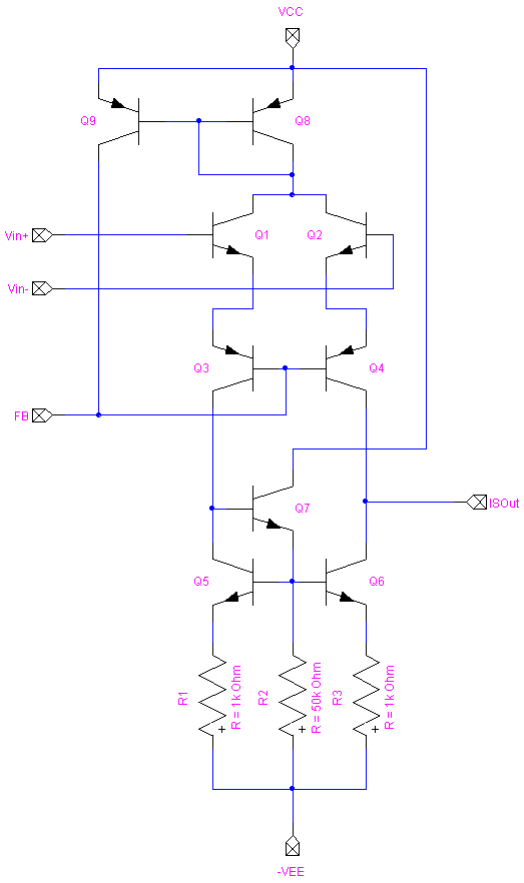


Figure 19 and Figure 19 show the internal circuitry of each sub-circuit block. As you can see the circuit is composed of bipolar junction transistors (BJTs), resistors and capacitor. The properties of the BJTs are given in their respective model statements.

Figure 18 Internal of each stage in UA741 (Part 1)

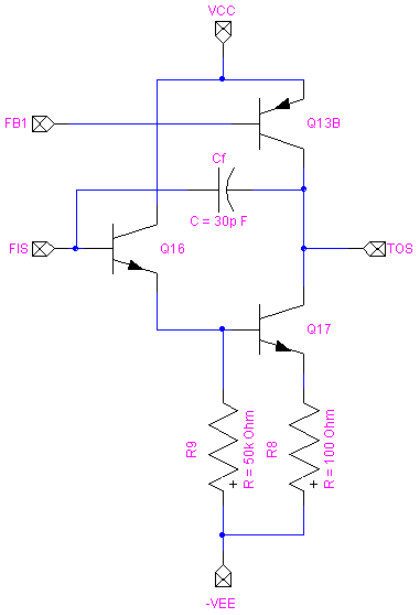


a. Bias

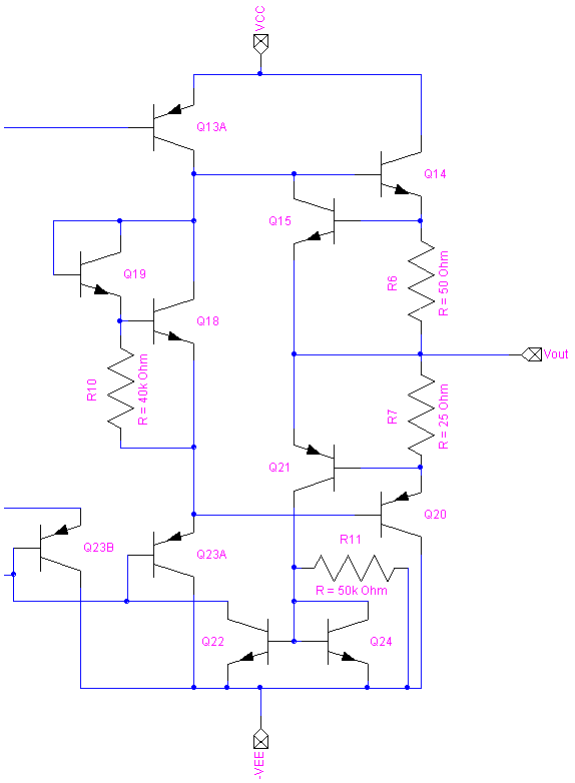


b. Input

Figure 19 Internal of each stage in UA741 (Part 2)



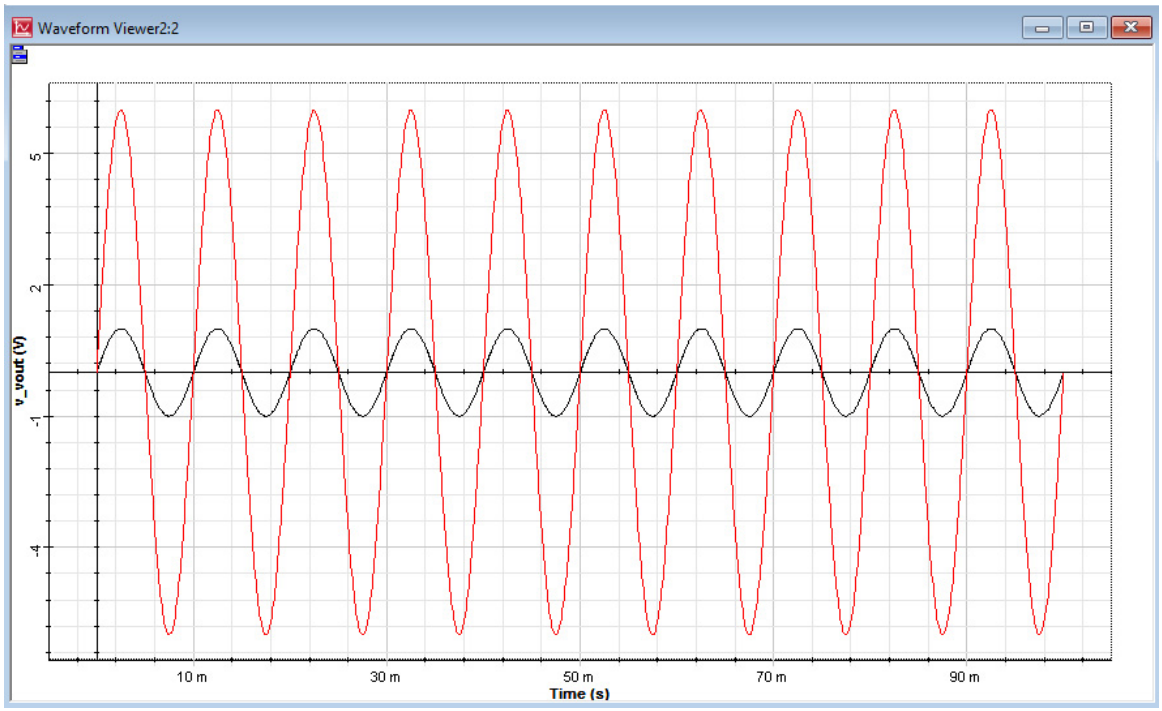
c. Intermediate



d. Output

Input and output voltage waveforms for the transient analysis are shown in Figure 20 where you can see the gain is 6 and the output is non-inverted.

Figure 20 Input (black) and output (red) waveforms



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