# Photonic-crystal-based all-optical NOT logic gate

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In the present paper, we have utilized the concept of photonic crystals for the implementation of an optical NOT gate inverter. The designed structure has a hexagonal arrangement of silicon rods in air substrate. The logic function is based on the phenomenon of the existence of the photonic bandgap and resulting guided modes in defect photonic crystal waveguides. We have plotted the transmission, extinction ratio, and tolerance analysis graphs for the structure, and it has been observed that the maximum output is obtained for a telecom wavelength of 1.554 μm. Dispersion curves are obtained using the plane wave expansion method, and the transmission is simulated using the finite element method. The proposed structure is applicable for photonic integrated circuits due to its simple structure and clear operating principle. © 2015 Optical Society of America

## 1. INTRODUCTION

The concept of the photonic crystal (PhC) was proposed by Eli Yablonovitch in 1987, and since then PhCs have attracted much attention as a possible platform for integrated photonic circuits, which play a role in electronics and communication [1,2]. PhCs have interesting properties such as the photonic bandgap (PBG), i.e., the range of frequencies that are not allowed to propagate into the PhC. PBG-induced waveguiding applications of such materials can be used for localization and trapping of light over a band of wavelengths [3–7]. The two-dimensional PhCs have a high refractive index contrast that plays an important role in controlling the propagation modes, accurate PBG calculation, efficient light confinement, simple design, and easy fabrication [8–11]. These structures have dimensions of the order of wavelengths of light for future photonic integrated circuits. The all-optical NOT gate forms a key element in next-generation optical computing, which includes optical signal processing such as binary addition, parity checking, and switching with high speeds. [12]. However, the reported work suffers from the limitations of a highly specific lattice constant, low transmitted power, and a low extinction ratio.

In the present paper, the design and analysis of a NOT gate based on a PhC is considered and investigated based on a hexagonal arrangement of silicon rods in air. Electromagnetic wave propagation was simulated using the finite element method (FEM), and the PBG has been calculated using plane wave expansion (PWE). Dispersion curves along line defect waveguides have been calculated to show the presence of guided modes corresponding to a telecom wavelength of 1.554 μm. The

distinction between logical "zero" and "one" is improved, and power consumption has also been reduced in this scheme. This structure has the potential to be applied in photonic integrated circuits.

## 2. STRUCTURE DESIGN

An optical NOT gate in PhC with a hexagonal arrangement of silicon ($n = 3.42$) rods in air is being designed. The designed NOT gate contains one input port (Port 1), one probe signal (Port 2), and one output port (Port 3), as can be observed from the schematic diagram in Fig. 1(a). The probe signal is given as an input for the operation of the NOT gate, works as control signal, and is always kept high. So, if the input signal at Port 1 is zero (0), the probe signal passes through the waveguide and makes the output high, i.e., 1. Similarly, in the second case, the probe signal is high, and when the input signal at Port 1 is 1, the probe signal and input signal interfere destructively and cause the output at Port 3 to be low, i.e., 0. Hence it satisfies the truth table (Table 1) of the NOT gate. The radius of the silicon rods is $r = 0.231$ μm, and lattice constant chosen is 0.68 μm. The selection of the radius of the holes of the designed structure is based upon the fact that a bandgap exists for the telecom wavelength 1.554 μm. The designed structure supports a large PBG for TE modes that varies in the normalized frequency range of $0.3863 \leq a/\lambda \leq 0.4899$, obtained using the PWE method as shown in Fig. 1(b). The range of the PBG can be varied by changing the radius of the silicon rods and the lattice constant for the proposed NOT gate. The input waveguide and output waveguide are formed by removing a few
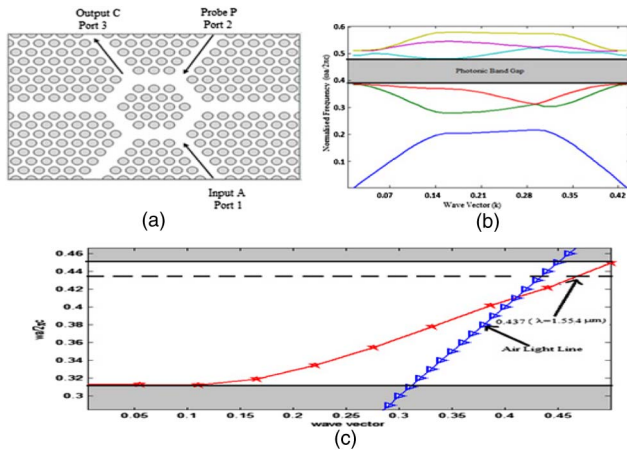
**Fig. 1.**    (a) Schematic diagram of the proposed NOT gate with silicon rods in air, (b) band structure for TE-like modes for a hexagonal lattice having a Si radius $r = 0.231$ μm, $a = 0.68$ μm, (c) dispersion diagram for photonic crystal silicon rods in air with $a = 0.68$ μm.

silicon rods from the direction of propagation. The line defect created supports the guided modes for the telecom wavelength within the input waveguide.

Figure 1(c) shows the guided mode at a normalized frequency of 0.437, which corresponds to a wavelength of 1.554 μm. The blue line in the figure is the air light line. Above the air light line, the waveguide modes are known as radiant modes, which are lossy in nature, whereas the modes below the light line are known as the guided modes.

## 3. TRANSMITTANCE

The transmittance (TR) of the designed NOT gate is defined as the ratio of the output power to the total input power, and mathematically it can be written as

$$TR = P_C/(P_A + P), \tag{1}$$

where $P_c$ is the power at logic output port C, and $P_A$ and $P$ are the powers at input port A and input probe signal P, respectively. For the input combination of $A = 0$ and probe equal to 1, the output is high (=1). Figure 2(a) shows the electric field distribution for the case where input is low, giving a high output. However, when the input combination of $A = 1$, $P = 1$ is taken, then the output becomes low (=0), which is because of the destructive interference of the input signal and probe signal
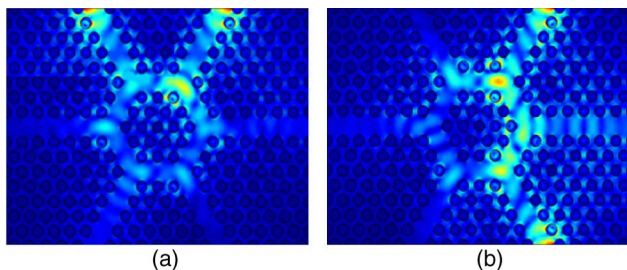


**Fig. 2.**    (a) Electric field distribution for $A = 0$, $P = 1$, (b) electric field distribution for $A = 1$, $P = 1$.

**Table 1.    Truth Table for NOT Gate**

| Input ($A$) | Probe ($P$) | Output |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 1 | 0 |

with each other, and the output becomes zero. Figure 2(b) shows the electric field distribution for both high inputs. Table 1 gives the corresponding truth table for the NOT gate.

Figure 3 shows the plot of the normalized transmission versus the wavelength for a NOT gate. The wavelength range taken here is for the C-Band, i.e., 1540–1560 nm. It is observed from the curve that the transmission increases with the wavelength, and the maximum output is obtained at 1554 nm.

## 4. EXTINCTION RATIO

The extinction ratio (ER) can be defined as

$$ER = 10 \log_{10}(P_1/P_0), \tag{2}$$

where $P_1$ is the power for logic 1 obtained at the output port and $P_0$ is the power for logic 0 obtained at the output port. The ER is used to describe the efficiency with which the transmitted optical power is modulated over the designed waveguide. The ER is inversely proportional to the bit error rate (BER). The BER can be defined as the ratio of the number of corrupted bits to the total number of transmitted bits [13]. So here we achieved a 10 dB extinction, which is fine for this designed structure. Figure 4 shows the ER for the NOT gate; the wavelength variation considered here is 1540–1560 nm.

## 5. TOLERANCE ANALYSIS

In this section we present the effect of change in the silicon rod radius on the transmission characteristics of the optimized optical NOT gate in PhC. We calculated the transmission changes for –2% to +2% variation in the radius of the silicon rods for a high output (=1), when the input is zero. It is observed from the tolerance curve (Fig. 5) that at a –2% change in radius, the transmission is nearly 50%, whereas at a +2% variation in radius, the transmission has been increased to 59%. It is observed from the tolerance analysis graph that from –1.4%
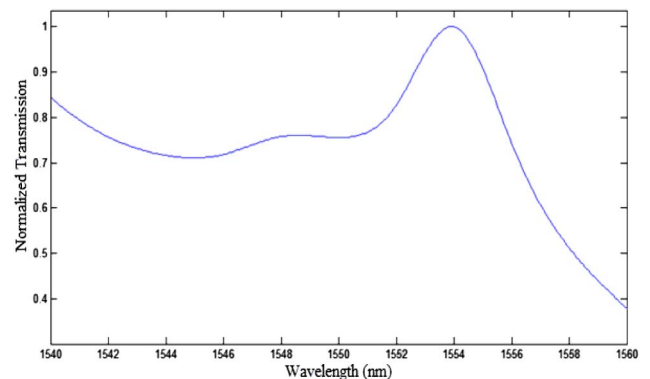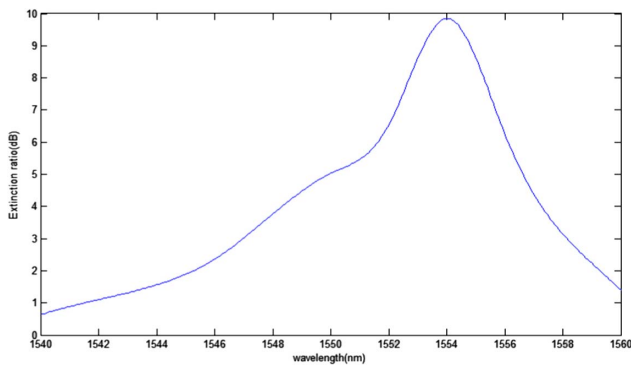


**Fig. 3.**    NOT gate transmission curve.

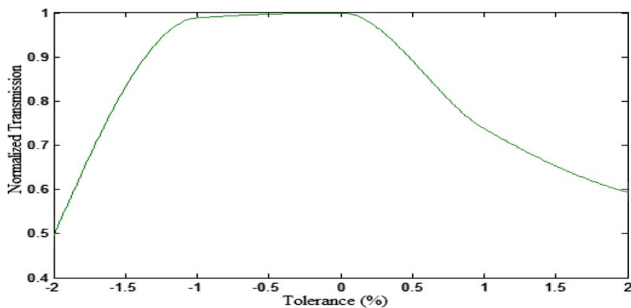**Fig. 4.**    NOT gate extinction ratio curve.



**Fig. 5.**    Effect of tolerances in radius ($r$) on the transmission characteristics of the proposed optimized optical NOT gate.

to 0.4%, no change in transmission takes place, which is an advantage while fabricating the structure. Tolerance analysis of the above factors leads us to conclude that the proposed optical NOT gate based on PhC has a reasonable fabrication tolerance.

## 6. RESULT AND DISCUSSION

Nanophotonics is a growing area in which photonic devices can be implemented at the nano level. Hence they are considered for analysis by researchers. The present paper explains the design and analysis of an all-optical NOT gate based on PhC with silicon rods in air. The optical NOT gate reported in this paper has low dimension as compared to the reported literature. The designed hexagonal-based structure is effective, and a high data rate can be achieved. Ghadrdan and Birjandi [14] designed a NOT gate with a square-based arrangement of Indium Phosphide rods in air with the dimensions 12 μm × 12 μm. However, the optical NOT gate designed in the present paper utilizes a hexagonal arrangement of silicon rods in air with the dimensions 12.9 μm × 9.4 μm. The silicon used in this work has more advantages, as it is utilized in the design and fabrication of the CMOS bipolar junction transistor used in electronics, unlike the indium phosphide rods used in [14]. Also, silicon is easily available and offers a wide temperature operating range, and the silicon rods in air structure provides more dielectric contrast, giving a wide range of the PBG as compared to indium phosphide rods in air, as reported in the literature

[14]. The transmission characteristics obtained show a maximum output at 1.554 μm. The ER has also been taken into consideration while doing the analysis and is found to be nearly 10 dB for the optical NOT gate designed. We have carried out the tolerance analysis of the device for a ±2% change in the radius of the silicon rods for the whole structure. It is found that the working wavelength region of the guided mode remains unaffected in the proposed optical NOT gate, with an increase or decrease in the defect radii by 2%, though there is a fall/increase in transmission accordingly. Liu *et al.* [11] used multi-mode interference and binary phase-shift keying (BPSK) for the implementation of logic gates. They utilized the finite-difference time-domain method for realizing the logical gates. Physically, the main limitation in realizing these structures occurs during the generation of the BPSK signals. One has to take care of the BPSK signals externally, whereas in our proposed structure, we have used the FEM and there is no requirement for BPSK signals. Hence it is far simpler then the previous method of realizing a NOT logic gate.

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